

10/581 754

(12) INTERNATIONAL APPLICATION PUBLISHED UNDER THE PATENT COOPERATION TREATY (PCT)

(19) World Intellectual Property Organization  
International Bureau



(43) International Publication Date  
12 July 2007 (12.07.2007)

PCT

(10) International Publication Number  
**WO 2007/076623 A1**

(51) International Patent Classification:  
*G06F 12/00* (2006.01)

Room 701, No. 8, Lane 199, Biyun Road, Pudong District, Shanghai (CN).

(21) International Application Number:  
PCT/CN2005/002385

(74) Agent: **INTELLECPRO CHINA LIMITED**; 11/F, Tower C, Five Buildings, 9 Chegongzhuang Dajie, Xicheng District, Beijing 100044 (CN).

(22) International Filing Date:  
30 December 2005 (30.12.2005)

(81) Designated States (*unless otherwise indicated, for every kind of national protection available*): AE, AG, AL, AM, AT, AU, AZ, BA, BB, BG, BR, BW, BY, BZ, CA, CH, CN, CO, CR, CU, CZ, DE, DK, DM, DZ, EC, EE, EG, ES, FI, GB, GD, GE, GH, GM, HR, HU, ID, IL, IN, IS, JP, KE, KG, KM, KN, KP, KR, KZ, LC, LK, LR, LS, LT, LU, LV, LY, MA, MD, MG, MK, MN, MW, MX, MZ, NA, NG, NI, NO, NZ, OM, PG, PH, PL, PT, RO, RU, SC, SD, SE, SG, SK, SL, SM, SY, TJ, TM, TN, TR, TT, TZ, UA, UG, US, UZ, VC, VN, YU, ZA, ZM, ZW.

(25) Filing Language: English

(26) Publication Language: English

(71) Applicant (*for all designated States except US*): **INTEL CORPORATION** [US/US]; 2200 Mission College Boulevard, Santa Clara, CA 95052 (US).

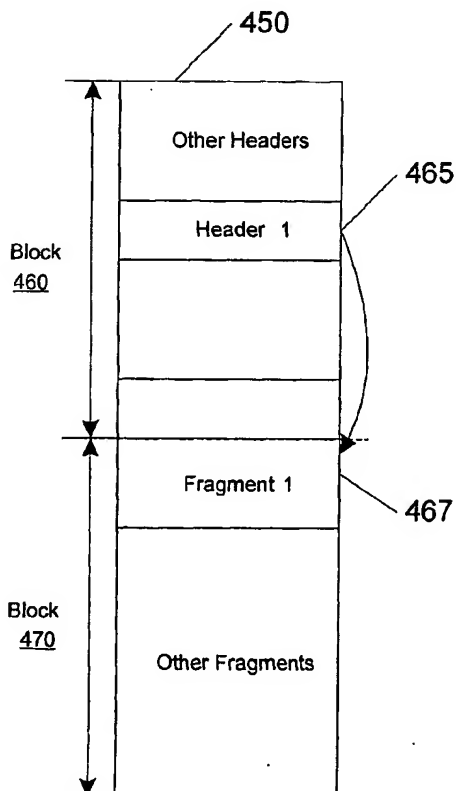
(84) Designated States (*unless otherwise indicated, for every kind of regional protection available*): ARIPO (BW, GH, GM, KE, LS, MW, MZ, NA, SD, SL, SZ, TZ, UG, ZM, ZW), Eurasian (AM, AZ, BY, KG, KZ, MD, RU, TJ, TM), European (AT, BE, BG, CH, CY, CZ, DE, DK, EE, ES, FI,

(72) Inventors; and

(75) Inventors/Applicants (*for US only*): **ZHENG, Cheng** [CN/CN]; Room 602, No 32, Lane 675, Gumei Road, Minhang District, Shanghai (CN). **WANG, Hongyu** [CN/CN];

[Continued on next page]

(54) Title: BIT-ALTERABLE NON-VOLATILE MEMORY MANAGEMENT



(57) Abstract: Methods and apparatuses for storage of data in bit-alterable, non-volatile memories. In some embodiments, an array of memory locations implemented as bit-alterable, non-volatile memory configured as a plurality of blocks of memory locations; and control circuitry coupled with the array of memory locations to cause a block of data to be stored in the array of memory spanning a boundary between a first block of memory locations and a second block of memory locations. One or more processors access system data during initialization of an electronic system by retrieving data from a pre-selected location in a bit-alterable, non-volatile memory without scanning multiple memory locations to locate the system data.

WO 2007/076623 A1



FR, GB, GR, HU, IE, IS, IT, LT, LU, LV, MC, NL, PL, PT,  
RO, SE, SI, SK, TR), OAPI (BF, BJ, CF, CG, CI, CM, GA,  
GN, GQ, GW, ML, MR, NE, SN, TD, TG).

**Published:**

— with international search report

**Declaration under Rule 4.17:**

— of inventorship (Rule 4.17(iv))

*For two-letter codes and other abbreviations, refer to the "Guidance Notes on Codes and Abbreviations" appearing at the beginning of each regular issue of the PCT Gazette.*